Abstract

An architecture for connection between regions in or adjacent a semiconductor layer. Generally, an integrated circuit structure, having a semiconductor layer with a major surface formed along a plane, includes first and second spaced-apart doped regions formed in the surface. A third doped region of different conductivity type than the first region is positioned over the first region. A conductive layer comprising a metal is formed between the first and second regions and above the surface plane, providing electrical connection between the doped regions.

According to one embodiment of the invention a semiconductor device includes a first layer of semiconductor material and a first field effect transistor having a first source/drain region formed in the first layer. A channel region of the transistor is formed over the first layer and an associated second source/drain region is formed over the channel region. The device includes a second field effect transistor also having a first source/drain region formed in the first layer. A channel region of the second transistor is formed over the first layer and an associated second source/drain region is formed over the channel region. A conductive layer comprising a metal is positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region.

In an associated method of manufacture a first device region, selected from the group consisting of a source region and a drain region of a field effect transistor, is formed on a semiconductor layer. A second device region, selected from the group consisting of a source region and a drain region of a field effect transistor, is also formed on the semiconductor layer. A conductor layer comprising metal is positioned adjacent the first and second device regions to effect electrical connection between the first and second device regions. A first field effect transistor gate region is formed over the first device region and the conductor layer and a second field effect transistor gate region is formed over the second device region and the conductor layer.

In another associated method for fabricating a semiconductor device a first device region, selected from the group consisting of a source region and a drain region of a field effect transistor, is formed on a semiconductor layer and a second device region, selected from the group consisting of a source region and a drain region of a field effect transistor

is also formed on the semiconductor layer. A conductor layer is positioned adjacent the first and second device regions to effect electrical connection between the first and second device regions. A first field effect transistor gate region is formed over the first device regions and the conductor layer and a second field effect transistor gate region is formed over the second device region and the conductor layer.

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